PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-018540
(43)Date of publication of application : 17.01.1997

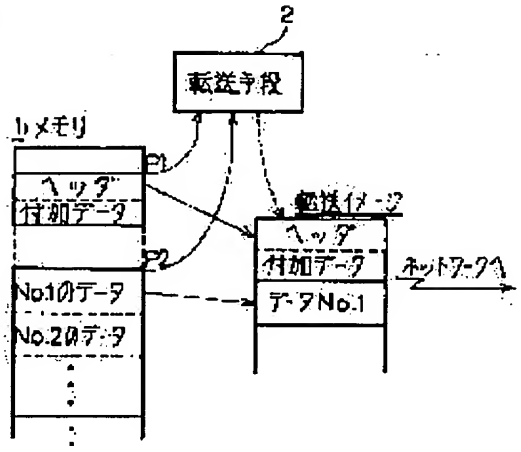
(51)Int.Cl. H04L 29/02

(21)Application number : 07-164907
(22)Date of filing : 30.06.1995

(71)Applicant : FUJITSU LTD
(72)Inventor : NISHIKAWA KATSUHIKO

(54) DATA TRANSFER SYSTEM

(57)Abstract:
PURPOSE: To eliminate unnecessary reading from and writing to a memory and to improve transfer speed by previously generating a header by writing dummy data so as to make an integral multiple of the number at the tail of 1st data.
CONSTITUTION: A transfer means 2 informed of the head address P1 of a header in a memory 1 and the head address of data reads the header and additional data (dummy data), written previously to an integral multiple of some number, out of the address P1 and transfers them to a network. Then the data are read out in blocks from the reported head address P2 of the data in the memory 1 while sectioned to an integral multiple of the certain number, and transferred to the network. Those are repeated to the end of the data. It is not necessary to read and write the data out and in the memory 1 to make blocks the integral multiple of the certain number like before, and the data can be transferred fast.



(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平9－18540

(43)公開日　平成９年(1997)１月17日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ		技術表示箇所
Ｈ０４Ｌ　29/02			Ｈ０４Ｌ　13/00	３０１Ａ	

審査請求　未請求　請求項の数３　ＯＬ　（全　５　頁）

(21)出願番号　特願平7－164907

(22)出願日　平成７年(1995)６月30日

(71)出願人　000005223
富士通株式会社
神奈川県川崎市中原区上小田中４丁目１番１号

(72)発明者　西川　克彦
神奈川県川崎市中原区上小田中1015番地
富士通株式会社内

(74)代理人　弁理士　岡田　守弘

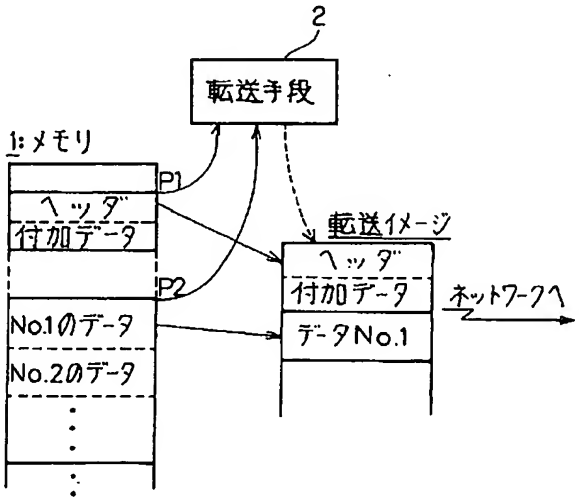
(54)【発明の名称】　データ転送システム

(57)【要約】

【目的】　本発明は、データをある数の整数倍にしチェインして転送するデータ転送システムに関し、第１のデータ（例えばヘッダ）の後部にある数の整数倍となるようにダミーデータを書き込んで作成し、この第１のデータと転送すべき第２のデータとをチェイニングして転送し、メモリ内で余分な読み書きの発生を無くし、転送速度の向上を図ることを目的とする。

【構成】　第１のデータの後部にある数の整数倍となるようにダミーデータを予め付加しておき、転送時にある数の整数倍のダミーデータの付加された第１のデータ、および第２のデータをある数の整数倍に区切ってチェインして転送する手段を備えるように構成する。

本発明の１実施例構成図



1

【特許請求の範囲】
【請求項１】データをある数の整数倍にしチェインして転送するデータ転送システムにおいて、
第１のデータの後部に当該第１のデータがある数の整数倍となるようにダミーデータを予め付加しておき、転送時にある数の整数倍のダミーデータの付加された第１のデータ、および第２のデータをある数の整数倍に区切ってチェインして転送する手段を備えたことを特徴とするデータ転送システム。
【請求項２】上記ダミーデータ中に転送しようとするデータ長を付加したことを特徴とする請求項１記載のデータ転送システム。
【請求項３】上記第１のデータをヘッダおよび第２のデータを転送しようとするデータとしたことを特徴とする請求項１あるいは請求項２記載のデータ転送システム。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、データをある数の整数倍にしチェインして転送するデータ転送システムに関するものである。
【０００２】ハードディスクなどの外部記憶装置に蓄積されたデータをネットワークを介して転送する場合、データの先頭にヘッダを付加してチェイニングを行う必要がある。このようなチェイニングが可能なネットワークのインタフェースチップなどにおいて、チェインされるデータの長さがある数の整数倍でないと動作しないという制限がある場合がある。この制限がある場合に、簡易かつ迅速にヘッダおよびデータのチェイニングを行うことが望まれている。
【０００３】
【従来の技術】従来のチェイニングの様子を図４に示す。図４は、従来技術の説明図を示す。
【０００４】まず、外部記憶装置であるディスク装置上のデータが一旦メモリ２１の②のように連続して読み込んで格納する。その後、転送単位毎に、予めメモリ２１の①の部分に書き込まれているヘッダを読み出して他のメモリ２１の③の部分に書き込み、これに続けて、②の部分のデータを読み出して丁度、ある数（例えば４８バイト）の整数倍となるように図中のデータＮｏ．１の一部を書き込む。そして、ヘッダと残ったデータをある数の整数倍となるように分割しチェイニングして転送するようにしていた。
【０００５】
【発明が解決しようとする課題】このため、ある数の整数倍のヘッダを作成する際に、ヘッダを読み出して他のメモリ上に書き込み、これに続けてデータの先頭から読み出して書き込んで、丁度ある数の整数倍としヘッダを作成した後、この作成したヘッダと、残りのデータをある数の整数倍に分割してチェイニングし、ネットワークを介して転送していたため、ヘッダを作成するためにメモリ内で読み出しと書き込みが発生してしまい、しかも、残りのデータついてある数の整数倍に分けてチェイニングをその都度行う必要があり、余分なメモリの読み書きなどが発生し、転送速度を低下させてしまうという問題がある。

2

【０００６】本発明は、これらの問題を解決するため、第１のデータ（例えばヘッダ）の後部にある数の整数倍となるようにダミーデータを書き込んで予めヘッダを作成しておき、この第１のデータと転送すべき第２のデータとをチェイニングして転送し、メモリ内で余分な読み書きの発生を無くし、転送速度の向上を図ることを目的としている。
【０００７】
【課題を解決するための手段】図１を参照して課題を解決するための手段を説明する。図１において、メモリ１は、転送しようとするヘッダやデータなどを格納するものである。
【０００８】転送手段２は、メモリ１からヘッダおよびデータを取り出してネットワークを介して宛先に転送するものである。
【０００９】
【作用】本発明は、図１に示すように、第１のデータであるヘッダの先頭アドレスＰ１および第２のデータである転送しようとするデータの先頭アドレスＰ２の通知に対応して、転送手段２が先頭アドレスＰ１からヘッダおよびある数の整数倍となるように予め付加されたダミーデータをまとめてブロックとしてネットワークに転送すると共に、続けて先頭アドレスＰ２からある数の整数倍となるようにブロックに分けてネットワークに転送するようにしている。
【００１０】この際、ヘッダ中のダミーデータに転送しようとするデータ長を付加し、転送するようにしている。また、第１のデータをヘッダおよび第２のデータを転送しようとするデータとし、転送するようにしている。
【００１１】従って、第１のデータである例えばヘッダの後部にある数の整数倍となるようにダミデータを書き込んで予め作成しておき、この第１のデータと転送すべき第２のデータをある数の整数倍となるように分割しチェイニングして転送することにより、従来のメモリ内で余分な読み書きなどの発生を無くし、転送速度を向上させることが可能となる。
【００１２】
【実施例】次に、図１から図３を用いて本発明の実施例の構成および動作を順次詳細に説明する。
【００１３】図１は、本発明の１実施例構成図を示す。図１において、メモリ１は、第１のデータであるヘッダおよび第２のデータである転送しようとするデータを格納しようとするものである。ここでは、アドレスＰ１からヘッダとこのヘッダに続けてある数の所定数倍となる

ように付加データを付加して格納する。また、アドレスＰ２から転送しようとするデータ（Ｎｏ．１、Ｎｏ．２・・・）を連続に格納する。

【００１４】次に、データの転送時の動作を説明する。

（１）　メモリ１中のヘッダの先頭アドレスＰ１およびデータの先頭アドレスＰ２の通知を受けた転送手段２は、アドレスＰ１からヘッダおよびある数の整数倍となるように予め書き込まれた付加データ（ダミーデータ）を読み出し、図示転送イメージのようにネットワークに転送する。

【００１５】（２）　続いて、通知を受けたメモリ１中のデータの先頭アドレスＰ２からデータをある数の整数倍となるように区切ってブロックとして読み出し、図示転送イメージのようにネットワークに転送することを、データが無くなるまで繰り返す。

【００１６】以上によって、ヘッダおよびこのヘッダに続いて付加データがある数の整数倍となるように予め書き込まれているため、転送手段２はヘッダの先頭アドレスＰ１およびデータの先頭アドレスＰ２の通知を受けると、そのまま図示の転送イメージのようにある数の整数倍のブロックにして順次ネットワークに転送でき、従来のメモリ１内である数の整数倍のブロックにするための読み書きが不要となり、高速にデータ転送することが可能となる。

【００１７】図２は、本発明のシステムブロック図を示す。図２において、外部記憶装置１１は、磁気ディスク装置などの外部記憶装置であって、ネットワークに転送しようとするデータを格納するものである。

【００１８】データＩ／Ｏ部１２は、後述する図３に記載するように、ヘッダ生成部１６で生成したヘッダおよびこのヘッダに続けてある数の整数倍となるように付加データをメモリ１中に書き込んだり、外部記憶装置１１から読み出したデータをメモリ１中の連続領域に書き込んだりするものである。

【００１９】送信部１３は、メモリ１からヘッダおよびデータをブロック（ある数の整数倍に区切ったデータ）毎に読み出してネットワークに送信するものである。ネットワーク１４は、送信部１３から送信されたデータ（パケット、フレームなど）を宛先に転送する網である。

【００２０】受信部１５は、ネットワーク１４を介して送信されてきたヘッダおよびデータを受信し、データを取り出して応用プログラムなどに渡すものである。次に、図３の説明図の順番に従い、図１および図２の構成の動作を詳細に説明する。

【００２１】図３は、本発明の動作説明図を示す。ここで、データＩ／Ｏ部１２、送信部１３、受信部１５、およびヘッダ生成部１６は、図２の同一番号のものと同一である。

【００２２】図３において、Ｓ１は、ヘッダを生成する。Ｓ２は、データ長を付加する。これは、Ｓ１で生成したヘッダに付加データを丁度、ある数（例えば４８バイト）の整数倍となるように付加する。

【００２３】Ｓ３は、メモリに書き込む。これは、Ｓ１およびＳ２で作成したヘッダおよび付加データをある数の整数倍にしたものを、例えば図１のメモリ１中にある数の整数倍としたヘッダおよび付加データを図示のように書き込む。

【００２４】Ｓ４は、データを読み込む。これは、外部記憶装置１１から送信しようとするデータを読み込む。Ｓ５は、メモリに書き込む。これは、Ｓ４で外部記憶装置１１から読み込んだデータを、例えば図１のメモリ１中の連続した領域に“Ｎｏ．１のデータ”、“Ｎｏ．２のデータ”というように順次書き込む。

【００２５】Ｓ６は、ヘッダ部のポインタを通知する。これは、Ｓ３でメモリ１に書き込んだヘッダおよび付加データの先頭アドレスＰ１を送信部１３に通知する。Ｓ７は、データ部のポインタを通知する。これは、Ｓ５でメモリ１に書き込んだデータの先頭アドレスＰ２を送信部１３に通知する。

【００２６】以上によって、データＩ／Ｏ部１２が指定された宛先に指定されたデータの転送指示を受けた場合に、ヘッダ生成部１６が生成した指定された宛先などからなるヘッダにある数の整数倍となるように付加データを付加してメモリ１に書き込むと共に、外部記憶装置１１から指定されたデータを読み出してメモリ１に書き込む。そして、ヘッダおよび付加データの先頭アドレスＰ１およびデータの先頭アドレスＰ２を送信部１３に通知して送信依頼する。これらにより、外部記憶装置１１から読み出したヘッダおよびデータをもとに、メモリ１上に読み書きの回数を最小限にして書き込み、送信準備が完了したこととなる。

【００２７】Ｓ８は、送信部１３がヘッダ／データを送信する。これは、Ｓ６およびＳ７で通知を受けたヘッダ部のポインタ（先頭アドレスＰ１）およびデータ部のポインタ（先頭アドレスＰ２）からそれぞれヘッダ（ヘッダ＋付加データ）およびデータを順次ネットワークに送信する。

【００２８】Ｓ９は、Ｓ８で送信されたヘッダを受信部１５が受信する。Ｓ１０は、データを受信する。これは、Ｓ９でヘッダを受信したことに続いて、データを受信する。

【００２９】Ｓ１１は、受信データ長＝データ長か判別する。これは、受信した受信データ長がヘッダに設定されたデータ長と等しいか判別する。ＹＥＳの場合には、全てのデータの受信済みと判明したので、一連の処理を終了する。一方、ＮＯの場合には、未だ受信してないデータがあると判明したので、Ｓ１０に戻り、データ受信を繰り返す。

【００３０】本実施例においては、ヘッダとデータをメ

5

モリ１に格納するとしたが、別々のメモリに格納してもよい。

【００３１】

【発明の効果】以上説明したように、本発明によれば、第１のデータ（例えばヘッダ）の後部にある数の整数倍となるように付加データを書き込んでおき、この第１のデータと転送すべき第２のデータを分割しチェイニングして転送する構成を採用しているため、従来のメモリ内で余分な読み書きの発生を無くし、転送速度の向上を図ることができる。

【図面の簡単な説明】

【図１】本発明の１実施例構成図である。

6

＊【図２】本発明のシステムブロック図である。

【図３】本発明の動作説明図である。

【図４】従来技術の説明図である。

【符号の説明】

１：メモリ

２：転送手段

１１：外部記憶装置

１２：データＩ／Ｏ部

１３：送信部

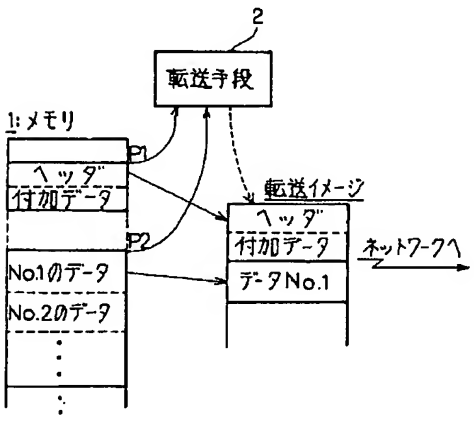
１４：ネットワーク

１５：受信部

１６：ヘッダ生成部

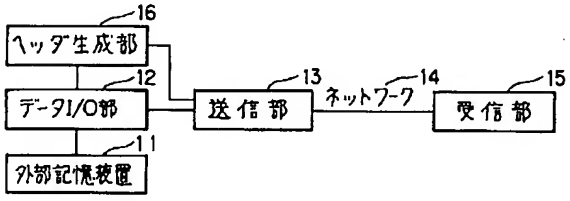
【図１】

本発明の１実施例構成図



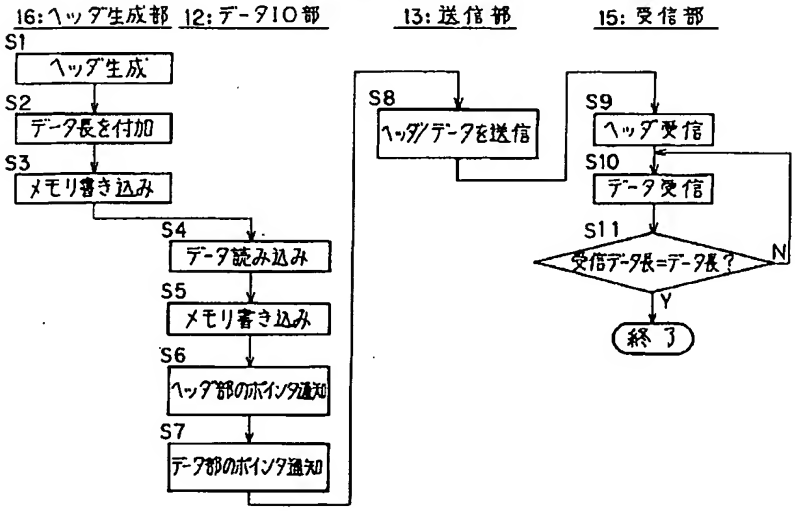
【図２】

本発明のシステムブロック図



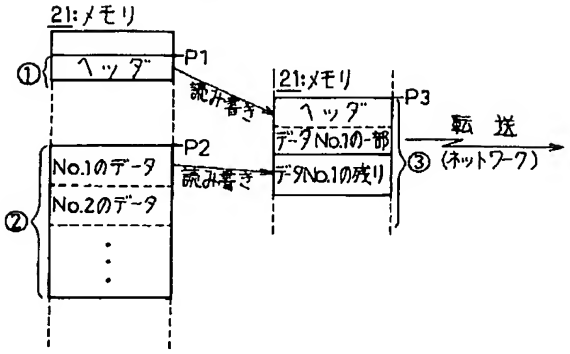
【図３】

本発明の動作説明図



【図４】

従来技術の説明図


21:メモリ
①
ヘッダ
P1
読み書き
21:メモリ
ヘッダ
P3
データNo.1の一部
転送
③
(ネットワーク)
P2
No.1のデータ
読み書き
データNo.1の残り
②
No.2のデータ

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-018540
(43)Date of publication of application : 17.01.1997

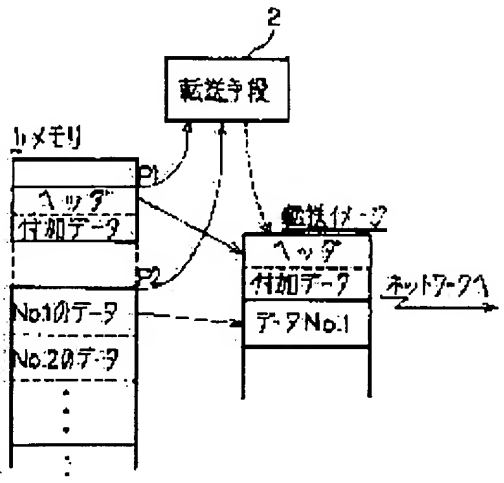
(51)Int.Cl. H04L 29/02

(21)Application number : 07-164907
(22)Date of filing : 30.06.1995

(71)Applicant : FUJITSU LTD
(72)Inventor : NISHIKAWA KATSUHIKO

(54) DATA TRANSFER SYSTEM

(57)Abstract:
PURPOSE: To eliminate unnecessary reading from and writing to a memory and to improve transfer speed by previously generating a header by writing dummy data so as to make an integral multiple of the number at the tail of 1st data.
CONSTITUTION: A transfer means 2 informed of the head address P1 of a header in a memory 1 and the head address of data reads the header and additional data (dummy data), written previously to an integral multiple of some number, out of the address P1 and transfers them to a network. Then the data are read out in blocks from the reported head address P2 of the data in the memory 1 while sectioned to an integral multiple of the certain number, and transferred to the network. Those are repeated to the end of the data. It is not necessary to read and write the data out and in the memory 1 to make blocks the integral multiple of the certain number like before, and the data can be transferred fast.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]In a data transfer system which makes data an integral multiple of a certain number, chains it, and transmits it, Dummy data is beforehand added so that it may become a number of integral multiples which have the 1st data concerned in the rear of the 1st data, A data transfer system provided with a means to divide into an integral multiple of a certain number the 1st data in which dummy data of a number of integral multiples which exist at the time of transmission was added, and the 2nd data, to chain them, and to transmit them.
[Claim 2]The data transfer system according to claim 1 adding data length which it is going to transmit in the above-mentioned dummy data.
[Claim 3]Claim 1 using the 1st data of the above as data which is going to transmit a header and the 2nd data, or the data transfer system according to claim 2.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention makes data the integral multiple of a certain number, and relates to the data transfer system chained and transmitted.
[0002]When transmitting the data stored in external storages, such as a hard disk, via a network, it is necessary to add a header to the head of data and to perform chaining. In the interface chip etc. of the network in which such chaining is possible, there may be restriction of not operating unless it is a number with the length of the data chained of integral multiples. When there is this restriction, to perform chaining of a header and data simply and promptly is desired.
[0003]
[Description of the Prior Art]The situation of the conventional chaining is shown in drawing 4. Drawing 4 shows the explanatory view of conventional technology.
[0004]First, the data on the disk unit which is an external storage once reads continuously like ** of the memory 21, and stores. Then, read the header currently beforehand written in the portion of ** of the memory 21 for every transfer unit, and it writes in the portion of ** of other memories 21, A part of data No.1 in a figure is written in so that the data of the portion of ** may be read and it may become an integral multiple of a certain number (for example, 48 bytes) exactly after this. And he divides and carries out chaining and was trying to transmit a header and the remaining data so that it may become an integral multiple of a certain number.
[0005]
[Problem(s) to be Solved by the Invention]For this reason, when creating the header of the integral multiple of a certain number, read a header and write in on other memories, and read from the head of data after this and it writes in, Since the remaining data was divided into the integral multiple of a certain number, chaining was carried out to this created header and it had transmitted via the network, after considering it as the integral multiple of a certain number exactly and creating a header, In order to create a header, read-out and writing occur within a memory, moreover it is necessary to divide into the integral multiple of the remaining numbers of data *********, and to perform chaining each time, reading and writing of an excessive memory, etc. occur, and there is a problem of reducing a transfer rate.
[0006]This invention writes in dummy data and creates the header beforehand so that it may become a number at the rear of the 1st data (for example, header) of integral multiples, in order to solve these problems, Chaining of this 1st data and the 2nd data that should be transmitted is carried out, it is transmitted, generating of excessive reading and writing is lost within a memory, and it aims at aiming at improvement in a transfer rate.
[0007]
[Means for Solving the Problem]With reference to drawing 1, The means for solving a technical problem is explained. In drawing 1, the memory 1 stores a header, data, etc. which it is going to

transmit.
[0008]The transfer means 2 takes out a header and data from the memory 1, and transmits them to an address via a network.
[0009]
[Function]This invention corresponds to the notice of the start address P2 of the data which is the start address P1 and the 2nd data of a header which are the 1st data and which it is going to transmit, as shown in drawing 1, Transmit collectively the dummy data added beforehand to a network as a block so that the transfer means 2 may serve as an integral multiple of a header and a certain number from the start address P1, and. He divides into a block and is trying to transmit to a network so that it may become an integral multiple of a certain number from the start address P2 continuously.
[0010]Under the present circumstances, he adds the data length which it is going to transmit to the dummy data in a header, and is trying to transmit. He uses the 1st data as the data which is going to transmit a header and the 2nd data, and is trying to transmit it.
[0011]Therefore, write in DAMIDETA and it creates beforehand so that it may become a number which is the 1st data of integral multiples which are in the rear of a header, for example, By dividing and carrying out chaining and transmitting this 1st data and the 2nd data that should be transmitted so that it may become an integral multiple of a certain number, generating of excessive reading and writing etc. is lost within the conventional memory, and it becomes possible to raise a transfer rate.
[0012]
[Example]Next, the composition and operation of the example of this invention are explained to details one by one using drawing 3 from drawing 1.
[0013]Drawing 1 shows 1 example lineblock diagram of this invention. In drawing 1, the memory 1 tends to store the data which is the header and the 2nd data which are the 1st data and which it is going to transmit. Here, attached data is added and stored so that it may become a number of predetermined number twice currently continued to a header and this header from the address P1. The data (No.1, No.2 ...) which it is going to transmit from the address P2 is stored in continuation.
[0014]Next, the operation at the time of a data transfer is explained.
(1) The transfer means 2 which received the notice of the start address P1 of the header in the memory 1, and the start address P2 of data, The attached data (dummy data) written in beforehand is read so that it may become an integral multiple of a header and a certain number from the address P1, and it transmits to a network like a graphic display transmission image.
[0015](2) Then, divide so that it may become an integral multiple of a certain number from the start address P2 of the data in the memory 1 which received the notice about data, read as a block, and repeat until data is lost [transmitting to a network like a graphic display transmission image, and].
[0016]Since it is beforehand written in so that it may become a number of integral multiples which have attached data following a header and this header by the above, If the notice of the start address P1 of a header and the start address P2 of data is received, the transfer means 2, The block of the integral multiple of a certain number is then used like the transmission image of a graphic display, it can transmit to a network one by one, the reading and writing for using the block of the integral multiple of the number which is in the conventional memory 1 become unnecessary, and it becomes possible to carry out data transfer at high speed.
[0017]Drawing 2 shows the system block figure of this invention. In drawing 2, the external storages 11 are external storages, such as a magnetic disk drive, and store the data which it is going to transmit to a network.
[0018]The data I/O part 12 writes in attached data into the memory 1 so that it may indicate to drawing 3 mentioned later and may become a number of integral multiples currently continued to the header generated by the header generating part 16, and this header, or, The data read from the external storage 11 is written in the continuation field in the memory 1.
[0019]The transmission section 13 reads a header and data from the memory 1 to every block (data

divided into the integral multiple of a certain number), and transmits to a network. The network 14 is a net which transmits the data (a packet, a frame, etc.) transmitted from the transmission section 13 to an address.

[0020]The receive section 15 receives the header and data which have been transmitted via the network 14, takes out data, and hands an application program etc. Next, according to the turn of the explanatory view of drawing 3, operation of the composition of drawing 1 and drawing 2 is explained in detail.

[0021]Drawing 3 shows the explanatory view of this invention of operation. Here, the data I/O part 12, the transmission section 13, the receive section 15, and the header generating part 16 are the same as that of the thing of the same number of drawing 2.

[0022]In drawing 3, S1 generates a header. S2 adds data length. Exactly, this adds attached data to the header generated by S1 so that it may become an integral multiple of a certain number (for example, 48 bytes).

[0023]S3 is written in a memory. This is written in like a graphic display of the header and attached data which made what made the header and attached data which were created by S1 and S2 the integral multiple of a certain number a number of integral multiples which are, for example in the memory 1 of drawing 1.

[0024]S4 reads data. This reads the data which it is going to transmit from the external storage 11. S5 is written in a memory. This writes the data read from the external storage 11 by S4 one by one like "the data of No.1", and "the data of No.2", for example in the continuous field in the memory 1 of drawing 1.

[0025]S6 notifies the pointer of a header unit. This notifies the transmission section 13 of the start address P1 of the header written in the memory 1 by S3, and attached data. S7 notifies the pointer of a data division. This notifies the transmission section 13 of the start address P2 of the data written in the memory 1 by S5.

[0026]When the data transfer directions specified as the address as which the data I/O part 12 was specified by the above are received, Add attached data and it writes in the memory 1 so that it may become a number in the header which consists of an address etc. which the header generating part 16 generated, and which were specified of integral multiples, and the data specified from the external storage 11 is read, and it writes in the memory 1. And the transmission section 13 is notified of the start address P1 of a header and attached data, and the start address P2 of data, and a transmission request is carried out. It means that the number of times of reading and writing is made into the minimum, and is written in on the memory 1 by these based on the header and data which were read from the external storage 11, and transmitting preparation was completed.

[0027]S8, the transmission section 13 transmits a header/data. This transmits a header (header + attached data) and data to a network one by one, respectively from the pointer (start address P1) of a header unit and the pointer (start address P2) of a data division which received the notice by S6 and S7.

[0028]The receive section 15 receives the header to which S9 was transmitted by S8. S10 receives data. This receives data after having received the header by S9.

[0029]S11 is distinguished in received-data length = data length. This distinguishes whether the received-data length which received is equal to the data length set as the header. Since finishing [reception of all the data] was turned out in YES, a series of processings are ended. Since it became clear that there is data which has not yet been received on the other hand in NO, it returns to S10 and data receiving is repeated.

[0030]In this example, although a header and data are stored in the memory 1, it may store in a separate memory.

[0031]

[Effect of the Invention]Attached data is written in so that it may become a number at the rear of the 1st data (for example, header) of integral multiples according to this invention, as explained

above, Since the composition which divides and carries out chaining of this 1st data and the 2nd data that should be transmitted, and transmits it is adopted, generating of excessive reading and writing can be eliminated within the conventional memory, and improvement in a transfer rate can be aimed at.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application]This invention makes data the integral multiple of a certain number, and relates to the data transfer system chained and transmitted.
[0002]When transmitting the data stored in external storages, such as a hard disk, via a network, it is necessary to add a header to the head of data and to perform chaining. In the interface chip etc. of the network in which such chaining is possible, there may be restriction of not operating unless it is a number with the length of the data chained of integral multiples. When there is this restriction, to perform chaining of a header and data simply and promptly is desired.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art]The situation of the conventional chaining is shown in drawing 4. Drawing 4 shows the explanatory view of conventional technology.
[0004]First, the data on the disk unit which is an external storage once reads continuously like ** of the memory 21, and stores. Then, read the header currently beforehand written in the portion of ** of the memory 21 for every transfer unit, and it writes in the portion of ** of other memories 21, A part of data No.1 in a figure is written in so that the data of the portion of ** may be read and it may become an integral multiple of a certain number (for example, 48 bytes) exactly after this. And he divides and carries out chaining and was trying to transmit a header and the remaining data so that it may become an integral multiple of a certain number.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention]Attached data is written in so that it may become a number at the rear of the 1st data (for example, header) of integral multiples according to this invention, as explained above, Since the composition which divides and carries out chaining of this 1st data and the 2nd data that should be transmitted, and transmits it is adopted, generating of excessive reading and writing can be eliminated within the conventional memory, and improvement in a transfer rate can be aimed at.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]For this reason, when creating the header of the integral multiple of a certain number, read a header and write in on other memories, and read from the head of data after this and it writes in, Since the remaining data was divided into the integral multiple of a certain number, chaining was carried out to this created header and it had transmitted via the network, after considering it as the integral multiple of a certain number exactly and creating a header, In order to create a header, read-out and writing occur within a memory, moreover it is necessary to divide into the integral multiple of the remaining numbers of data **********, and to perform chaining each time, reading and writing of an excessive memory, etc. occur, and there is a problem of reducing a transfer rate.
[0006]This invention writes in dummy data and creates the header beforehand so that it may become a number at the rear of the 1st data (for example, header) of integral multiples, in order to solve these problems, Chaining of this 1st data and the 2nd data that should be transmitted is carried out, it is transmitted, generating of excessive reading and writing is lost within a memory, and it aims at aiming at improvement in a transfer rate.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem]With reference to drawing 1, The means for solving a technical problem is explained. In drawing 1, the memory 1 stores a header, data, etc. which it is going to transmit.
[0008]The transfer means 2 takes out a header and data from the memory 1, and transmits them to an address via a network.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

OPERATION

[Function]This invention corresponds to the notice of the start address P2 of the data which is the start address P1 and the 2nd data of a header which are the 1st data and which it is going to transmit, as shown in drawing 1, Transmit collectively the dummy data added beforehand to a network as a block so that the transfer means 2 may serve as an integral multiple of a header and a certain number from the start address P1, and. He divides into a block and is trying to transmit to a network so that it may become an integral multiple of a certain number from the start address P2 continuously.
[0010]Under the present circumstances, he adds the data length which it is going to transmit to the dummy data in a header, and is trying to transmit. He uses the 1st data as the data which is going to transmit a header and the 2nd data, and is trying to transmit it.
[0011]Therefore, write in DAMIDETA and it creates beforehand so that it may become a number which is the 1st data of integral multiples which are in the rear of a header, for example, By dividing and carrying out chaining and transmitting this 1st data and the 2nd data that should be transmitted so that it may become an integral multiple of a certain number, generating of excessive reading and writing etc. is lost within the conventional memory, and it becomes possible to raise a transfer rate.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example]Next, the composition and operation of the example of this invention are explained to details one by one using drawing 3 from drawing 1.
[0013]Drawing 1 shows 1 example lineblock diagram of this invention. In drawing 1, the memory 1 tends to store the data which is the header and the 2nd data which are the 1st data and which it is going to transmit. Here, attached data is added and stored so that it may become a number of predetermined number twice currently continued to a header and this header from the address P1. The data (No.1, No.2---) which it is going to transmit from the address P2 is stored in continuation.
[0014]Next, the operation at the time of a data transfer is explained.
(1) The transfer means 2 which received the notice of the start address P1 of the header in the memory 1, and the start address P2 of data, The attached data (dummy data) written in beforehand is read so that it may become an integral multiple of a header and a certain number from the address P1, and it transmits to a network like a graphic display transmission image.
[0015](2) Then, divide so that it may become an integral multiple of a certain number from the start address P2 of the data in the memory 1 which received the notice about data, read as a block, and repeat until data is lost [transmitting to a network like a graphic display transmission image, and].
[0016]Since it is beforehand written in so that it may become a number of integral multiples which have attached data following a header and this header by the above, If the notice of the start address P1 of a header and the start address P2 of data is received, the transfer means 2, The block of the integral multiple of a certain number is then used like the transmission image of a graphic display, it can transmit to a network one by one, the reading and writing for using the block of the integral multiple of the number which is in the conventional memory 1 become unnecessary, and it becomes possible to carry out data transfer at high speed.
[0017]Drawing 2 shows the system block figure of this invention. In drawing 2, the external storages 11 are external storages, such as a magnetic disk drive, and store the data which it is going to transmit to a network.
[0018]The data I/O part 12 writes in attached data into the memory 1 so that it may indicate to drawing 3 mentioned later and may become a number of integral multiples currently continued to the header generated by the header generating part 16, and this header, or, The data read from the external storage 11 is written in the continuation field in the memory 1.
[0019]The transmission section 13 reads a header and data from the memory 1 to every block (data divided into the integral multiple of a certain number), and transmits to a network. The network 14 is a net which transmits the data (a packet, a frame, etc.) transmitted from the transmission section 13 to an address.
[0020]The receive section 15 receives the header and data which have been transmitted via the network 14, takes out data, and hands an application program etc. Next, according to the turn of the explanatory view of drawing 3, operation of the composition of drawing 1 and drawing 2 is explained in detail.

[0021]Drawing 3 shows the explanatory view of this invention of operation. Here, the data I/O part 12, the transmission section 13, the receive section 15, and the header generating part 16 are the same as that of the thing of the same number of drawing 2.
[0022]In drawing 3, S1 generates a header. S2 adds data length. Exactly, this adds attached data to the header generated by S1 so that it may become an integral multiple of a certain number (for example, 48 bytes).
[0023]S3 is written in a memory. This is written in like a graphic display of the header and attached data which made what made the header and attached data which were created by S1 and S2 the integral multiple of a certain number a number of integral multiples which are, for example in the memory 1 of drawing 1.
[0024]S4 reads data. This reads the data which it is going to transmit from the external storage 11. S5 is written in a memory. This writes the data read from the external storage 11 by S4 one by one like "the data of No.1", and "the data of No.2", for example in the continuous field in the memory 1 of drawing 1.
[0025]S6 notifies the pointer of a header unit. This notifies the transmission section 13 of the start address P1 of the header written in the memory 1 by S3, and attached data. S7 notifies the pointer of a data division. This notifies the transmission section 13 of the start address P2 of the data written in the memory 1 by S5.
[0026]When the data transfer directions specified as the address as which the data I/O part 12 was specified by the above are received, Add attached data and it writes in the memory 1 so that it may become a number in the header which consists of an address etc. which the header generating part 16 generated, and which were specified of integral multiples, and the data specified from the external storage 11 is read, and it writes in the memory 1. And the transmission section 13 is notified of the start address P1 of a header and attached data, and the start address P2 of data, and a transmission request is carried out. It means that the number of times of reading and writing is made into the minimum, and is written in on the memory 1 by these based on the header and data which were read from the external storage 11, and transmitting preparation was completed.
[0027]S8, the transmission section 13 transmits a header/data. This transmits a header (header + attached data) and data to a network one by one, respectively from the pointer (start address P1) of a header unit and the pointer (start address P2) of a data division which received the notice by S6 and S7.
[0028]The receive section 15 receives the header to which S9 was transmitted by S8. S10 receives data. This receives data after having received the header by S9.
[0029]S11 is distinguished in received-data length = data length. This distinguishes whether the received-data length which received is equal to the data length set as the header. Since finishing [reception of all the data] was turned out in YES, a series of processings are ended. Since it became clear that there is data which has not yet been received on the other hand in NO, it returns to S10 and data receiving is repeated.
[0030]In this example, although a header and data are stored in the memory 1, it may store in a separate memory.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is 1 example lineblock diagram of this invention.
[Drawing 2]It is a system block figure of this invention.
[Drawing 3]It is an explanatory view of this invention of operation.
[Drawing 4]It is an explanatory view of conventional technology.
[Description of Notations]
1: Memory
2: Transfer means
11: External storage
12: Data I/O part
13: Transmission section
14: Network
15: Receive section

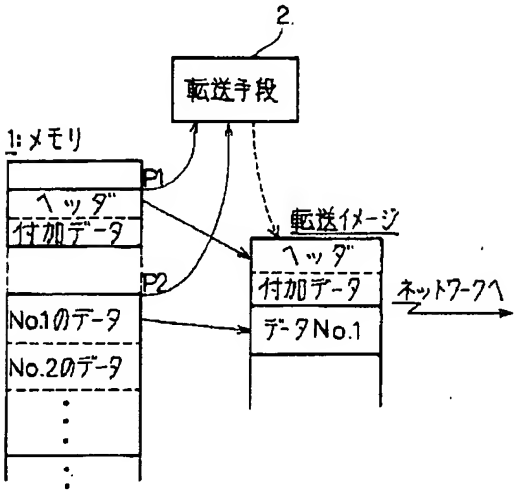
[Translation done.]

* NOTICES *

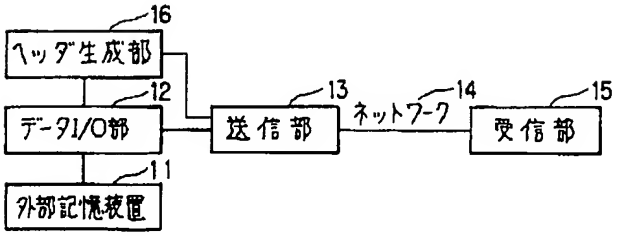
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]
本発明の1実施例構成図

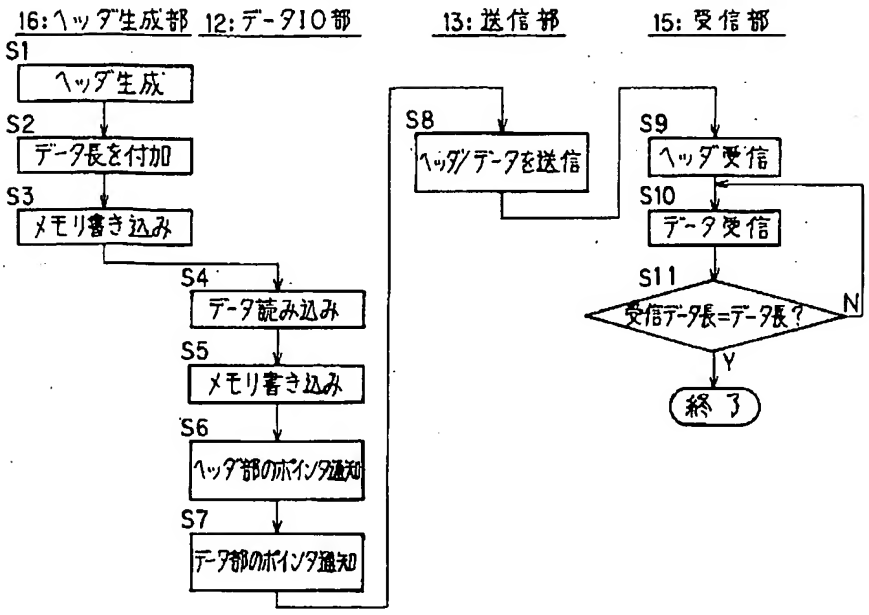


[Drawing 2]
本発明のシステムブロック図



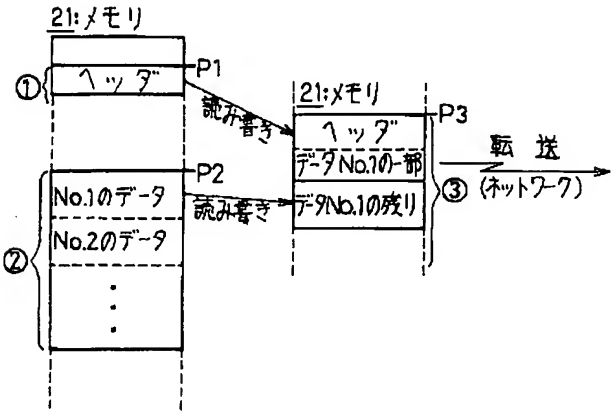
[Drawing 3]

本発明の動作説明図



[Drawing 4]

従来技術の説明図



[Translation done.]